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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,583	06/24/2003	Thomas Feudel	2000.106100	1209

7590 05/04/2004

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EXAMINER
BREWSTER, WILLIAM M

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 05/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,583	FEUDEL ET AL.	
	Examiner	Art Unit	
	William M. Brewster	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 3-9, 11-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Brady et al., U.S. Patent No. 6,638,832 B2.

Brady anticipates a method of forming, at least one field effect transistor on a semiconductive substrate, the method comprising forming, in fig. 5 an insulating film 520 on a surface of said substrate 510;

limitations from claims 6, 13: wherein said substrate comprises one of silicon and germanium or a combination thereof, silicon, col. 5, lines 8-17;

generating a strained surface layer at the interface of said insulating film and said substrate by implanting ions 522 comprised of at least one heavy inert material

limitations from claims 2, 9: wherein ions of at least one of xenon, argon, germanium, silicon, or a combination thereof are implanted: germanium;

limitations from claims 4, 11: wherein the implanting dose is in the range of approximately $10^{13}/cm^2$ - $10^{16}/cm^2$: $10^{14}/cm^2$ - $10^{16}/cm^2$, col. 5, lines 18-46;

limitations from claims 5, 12: wherein a thermal budget is adjusted to substantially avoid the grid restoration of said substrate: RTP is too short to fully restore a grid system, col. 5, lines 47-57;

through the gate insulating film into said substrate; and forming a gate insulating structure;

limitations from claims 7, 14: wherein said field effect transistor is one of an NMOS, a PMOS and a CMOS transistor: CMOS, col. 5, lines 58-65;

limitations from claim 15: wherein said insulating film comprises oxide, the method further comprising patterning said insulating film to form said gate insulating film and forming a gate polysilicon structure on said gate insulating film, inherent to forming well known CMOS process techniques, col. 5, lines 58-65.

Claims 1, 3, 8, 10, 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Dennison et al., U.S. Patent No. 5,650,350.

Dennison anticipates a method of forming at least one field effect transistor on a semiconductive substrate, in fig. 6, the method comprising forming an insulating film 102 on a surface of said substrate; in fig. 7, generating a strained surface layer at the interface of said insulating film and said substrate by implanting ions comprised of at least one heavy inert material through the gate insulating film into said substrate: germanium, col. 8, lines 8-23;

limitations from claims 3, 10: wherein the implanting energy is in the range of

approximately 20-100 or 200 keV: 50-200 keV, col. 8, lines 23-31;

and, in fig. 17, forming a gate insulating structure 134;

limitations from claim 16: in fig. 10, further comprising removing said insulating film after generating said strained layer, col. 8, lines 34-36, in fig. 14, forming a gate insulating layer 134 and, in fig. 16, patterning said gate insulating layer to form said insulating gate structure, col. 9, lines 8-15.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William M. Brewster whose telephone number is 571-272-1854. The examiner can normally be reached on Full Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

William M. Brewster

30 April 2004
WB